



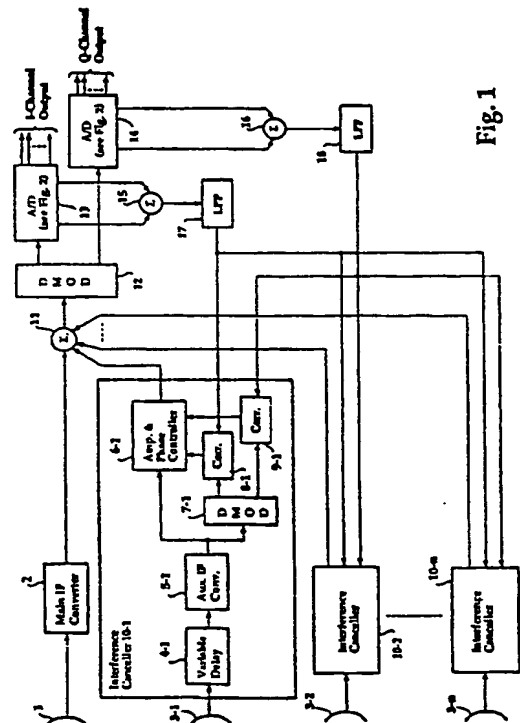
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coincident at the summing circuit.



Demodulator With Multiple Interference Cancellers Responsive To Correlations Between Undesired Signals and Error Signals

The present invention relates generally to demodulators for digital radio communications systems, and more specifically to interference cancellation for cancelling interfering signals from undesired multiple sources.

According to a prior art interference cancellation technique as described in Japanese Patent 62-16580, an auxiliary antenna is employed for detecting undesired signal, which is supplied to a correlator and an amplitude and phase controller to produce a cancelling signal. Desired signal is detected by the mainlobe of a main antenna. The output of the main antenna is fed to a summing amplifier where it is combined with the cancelling signal to cancel the undesired signal which is also detected by a sidelobe of the main antenna. To derive the cancelling signal, correlation is detected between the outputs of the main and auxiliary antennas by the correlator and used as an input to the controller to modify the output of the auxiliary antenna both in amplitude and phase. Being derived from correlation between the undesired signals detected by the main and auxiliary antennas, the signal-to-noise ratio of the interference cancelling signal is not sufficient to cancel interference, particularly when it is desired to cancel interfering signals coming from multiple sources. Further, in cases where the desired signal is also detected by a sidelobe of the auxiliary antenna, the correlation between it and the desired signal on the main path will be detected by the correlator. Such correlation would act in a way to decrease the desired signal.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a demodulator having a plurality of interference cancellers which respond to correlations between undesired signals from auxiliary antennas and error signals derived from the output of a main antenna.

According to the present invention, the demodulator comprises a main antenna having a main lobe for detecting a desired signal and sidelobes by which undesired signals may also be detected as interfering components. The output of the main antenna is converted to an intermediate frequency and supplied to a summing circuit where it is summed with plural interference cancelling signals. The output of the summing circuit is applied to a main quadrature demodulator for decomposing it into a first baseband component and

a second baseband component. A first decision circuit having multiple thresholds makes a decision on whether the first baseband component exceeds each of the multiple thresholds, and produces a multibit code as a first channel output and a first error signal in accordance with the decision. A second decision circuit having multiple thresholds makes a decision on whether the second baseband component exceeds each of the last-mentioned multiple thresholds, and produces a multibit code as a second channel output and a second error signal in accordance with the last-mentioned decision. A plurality of auxiliary antennas respectively detect the undesired signals and respectively feed auxiliary frequency converters for translating the frequency of the respective output of the auxiliary antennas to the intermediate frequency. A plurality of auxiliary quadrature demodulators are provided for respectively decomposing the output of each auxiliary frequency converter into first and second baseband components. A plurality of pairs of first and second correlators are provided so that the first correlators respectively detect correlations between the first baseband components and the first error signal, and the second correlators respectively detect correlations between the second baseband components and the second error signal. A plurality of amplitude and phase controllers are associated respectively with the first and second correlators of a respective one of the pairs for controlling the outputs of the auxiliary frequency converters in response to the outputs of the associated first and second correlators to generate the interference cancelling signals. Variable length delay lines are associated respectively with the auxiliary antennas for introducing respective delays so that the interference cancelling signals and corresponding interfering components contained in the output of the main frequency converter are time-coincident at the summing circuit.

Since the amplitude and phase control signals are derived from correlations between signals detected by the auxiliary antennas and the error signals from the decision circuits, the signal-to-noise ratios of such control signals are sufficient to cancel multiple interfering signals and no harmful effect occurs on the desired signal even if it is detected by the auxiliary antennas.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in fur-

ther detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of an embodiment of the present invention;

Fig. 2 is a block diagram of each A/D converter of Fig. 1;

Fig. 3 is a symbolic representation of the Fig. 1 embodiment for adjusting delay lines;

Fig. 4 is a block diagram of an alternative embodiment of the invention;

Fig. 5 is a symbolic representation of the Fig. 1 embodiment for adjusting delay lines associated with the embodiment of Fig. 4; and

Fig. 6 is a block diagram of another embodiment using a modified antenna system.

DETAILED DESCRIPTION

Referring now to Fig. 1, there is shown a digital modulator according to an embodiment of the present invention. The demodulator comprises a main antenna 1 and a plurality of auxiliary antennas 3-1 to 3-n. The main lobe of antenna 1 is so oriented that it receives incoming PSK or QAM signals from a desired transmitter station and its side lobes detect signals from a number of undesired interference sources. The output of antenna 1, containing both desired and undesired signals, is applied to a main IF converter 2 for intermediate frequency translation and coupled to a summing amplifier 11 where it is summed with interference cancelling signals. The output of summing amplifier 11 is applied to a quadrature demodulator 12 where the incoming signals are decomposed into an in-phase component and a quadrature component and supplied respectively as I-channel and Q-channel baseband signals to analog-to-digital converters 13 and 14.

As shown in Fig. 2, each of the analog-to-digital converters 13 and 14 includes a plurality of comparators 20, each of which compares the amplitude of the respective channel signal with one of successively increasing decision thresholds to make a decision in favor of logic-1 when the respective threshold is exceeded or in favor of logic-0 when the threshold is not exceeded. The outputs of comparators 20 are coupled to a logic circuit 23 to provide a multibit digital code as an I- or Q-channel output. Comparators 21 and 22 are provided to detect signals that exceed beyond the upper and lower limits of the specified decision thresholds and produce error bits for application to an adder 15 or 16.

Returning to Fig. 1, the error outputs of A/D converter 13 are summed by adder 15 and fed to a low-pass filter 17 to produce a phase error signal in

analog form, while the error outputs of A/D converter 14 are summed by adder 16 and fed to a low-pass filter 18 to produce an analog amplitude error signal.

On the other hand, auxiliary antennas 3-1 to 3-n have their main lobes respectively so oriented to detect signals from the interference sources. The signal from the desired transmitter station may also be detected by the auxiliary antennas. The outputs of auxiliary antennas 3-1 through 3-n are coupled respectively to interference cancellers 10-1 through 10-n of identical circuitry. For purposes of simplicity, only one interference canceller 10-1 is shown in detail.

Interference canceller 10-1 comprises a variable length delay line 4-1 through which the output of antenna 3-1 is coupled to an auxiliary IF converter 5-1 for translation to intermediate frequency. The output of IF converter 5-1 is applied to an amplitude and phase controller 6-1 as well as to a quadrature demodulator 7-1. The IF version of the undesired signal detected by antenna 3-1 is decomposed into an I-channel baseband signal and a Q-channel baseband signal. The I-channel component of the undesired signal is supplied to a correlator 8-1 to detect the correlation with a phase error contained in the output of low-pass filter 17, while the Q-channel component of the undesired signal is supplied to a correlator 9-1 to detect the correlation with an amplitude error contained in the output of low-pass filter 18. The outputs of correlators 8-1 and 9-1 are supplied to amplitude and phase controller 6-1 to respectively control the phase and amplitude of the undesired IF signal. The output of amplitude and phase controller 6-1 is an interference cancelling signal and is applied to the summing amplifier 11 to which the outputs of other cancellers 3-2 to 3-n are also applied. The undesired signal on the main path and the cancelling signal are of substantially equal magnitude, but of opposite phase at the summing amplifier 11 to cancel the interference.

The variable delay line 4-1 is manually adjusted to introduce a delay time so that the interference cancelling signal of canceller 10-1 and the corresponding undesired signal detected by the main antenna 1 arrive at the same time at the respective inputs of summing amplifier 11. As illustrated in Fig. 3, the variable delay line 4-1 is adjusted to introduce a path length C_1 so that the total of the electrical length L_1 from an interference source 30-1 to antenna 3-1 plus the electrical length S_1 from antenna 3-1 with the added electrical length C_1 to the summing amplifier 11 is equal to the total of the electrical length L_1 from the interference source 30-1 to antenna 1 plus the electrical length M from main antenna 1 to the summing amplifier 11. The phase difference due to

path length difference between the main path and the canceller 10-1 can be reduced to a minimum with this delay adjustment, and the phase difference due to a time-varying factor can be compensated for by the output of correlator 8-1.

Even if the source of desired signal is located in such a position that the desired signal is also detected by antenna 3-1 and time-coincident with the desired signal on the main electrical at the summing amplifier 11, no harmful effect occurs since the signals from the low-pass filters 17 and 18 are both indicative of errors.

Likewise, the variable length delay line of interference canceller 10-2 is independently adjusted to introduce an additional electrical length C_2 so that so that the total of the electrical length L_2 from an interference source 30-2 to antenna 3-2 plus the electrical length S_2 from antenna 3-2 with the added electrical length C_2 to the summing amplifier 11 is equal to the total of the electrical length L_2 from the interference source 30-2 to antenna 1 plus the electrical length M from antenna 1 to the summing amplifier 11. In this way, the interfering signals from sources 30-2 through 30-n can also be precisely cancelled at the summing amplifier 11 by the outputs of the individual cancellers 10-2 through 10-n.

Fig. 4 is an illustration of an alternative embodiment of the present invention which differs from the previous embodiment in that it replaces the summing amplifier 11 with a series of cascaded summing amplifiers 11-1 through 11-n provided respectively for the cancellers 10-1 to 10-n. Multiple undesired signals from sources 30-1 through 30-n are cancelled respectively at the summing amplifiers 11-1 through 11-n by respectively adjusting the delay lines of cancellers 10-1 through 10-n to introduce an electrical length C_i so that $L_i + M_i$ equals $L_i + S_i + C_i$ (where $i = 1, 2, \dots, n$) as shown in Fig. 5.

Instead of using separate auxiliary antennas 3, an arrangement shown in Fig. 6 can be advantageously employed in the present invention. In this embodiment, the antenna system comprises a parabolic reflector 40 upon which all incoming radio signals are reflected, a main feeder 41 and a plurality of auxiliary feeders 42-1 through 42-n. Main feeder 41 is oriented to detect one of the reflected signals which is desired and the auxiliary feeders are respectively oriented to detect undesired signals. The output of main feeder 41 is connected to the main IF converter 2, and the outputs of auxiliary feeders 42-1 through 42-n are connected respectively to the inputs of interference cancellers 10-2 through 10-n.

The foregoing description shows only preferred embodiments of the present invention. Various modifications are apparent to those skilled in the

art without departing from the scope of the present invention which is only limited by the appended claims. Therefore, the embodiments shown and described are only illustrative, not restrictive.

Claims

1. A demodulator comprising:

a main antenna having a main lobe for detecting a desired signal and sidelobes by which undesired signals may also be detected as interfering components;

a main frequency converter for translating the frequency of the output of said main antenna to an intermediate frequency;

summing means for summing the output of said main frequency converter with interference cancelling signals;

a main quadrature demodulator for decomposing the output of said summing means into a first main baseband component and a second main baseband component;

first decision means having multiple thresholds for making a decision on whether said first main baseband component exceeds each of said multiple thresholds, and producing a multibit code as a first channel output and a first error signal in accordance with said decision;

second decision means having multiple thresholds for making a decision on whether said second main baseband component exceeds each of the last-mentioned multiple thresholds, and producing a multibit code as a second channel output and a second error signal in accordance with the last-mentioned decision;

a plurality of auxiliary antennas for respectively detecting said undesired signals;

a plurality of auxiliary frequency converters for translating the frequency of the respective output of the auxiliary antennas to said intermediate frequency;

a plurality of auxiliary quadrature demodulators for respectively decomposing the output of each of said auxiliary frequency converters into first and second auxiliary baseband components;

a plurality of pairs of first and second correlators, the first correlators respectively detecting correlations between said first auxiliary baseband components and said first error signal, and said second correlators respectively detecting correlations between said second auxiliary baseband components and said second error signal;

a plurality of amplitude and phase control means associated respectively with the first and second correlators of a respective one of said pairs for controlling the outputs of said auxiliary frequency converters in response to the outputs of the asso-

ciated first and second correlators to generate said interference cancelling signals; and
a plurality of variable length delay lines associated respectively with said auxiliary antennas for introducing respective delays so that said interference cancelling signals and corresponding interfering components contained in the output of said main frequency converter are time-coincident at said summing means.

2. A demodulator as claimed in claim 1, wherein said summing means comprises a series of summing amplifiers cascaded between said main frequency converter and said main quadrature modulator, said summing amplifiers respectively receiving said interference cancelling signals, said variable length delay lines introducing respective delays so that said interfering cancelling signals and corresponding interfering components contained in the output of said main frequency converter are time-coincident at said respective summing amplifiers.

3. A demodulator as claimed in claim 1 or 2, wherein said main antenna and said auxiliary antennas comprise a parabolic reflector for reflecting said desired signal and said undesired signals, a main feeder oriented to detect the desired signal reflected off said parabolic reflector, and a plurality of auxiliary feeders oriented respectively for detecting the undesired signals reflected off said parabolic reflector.

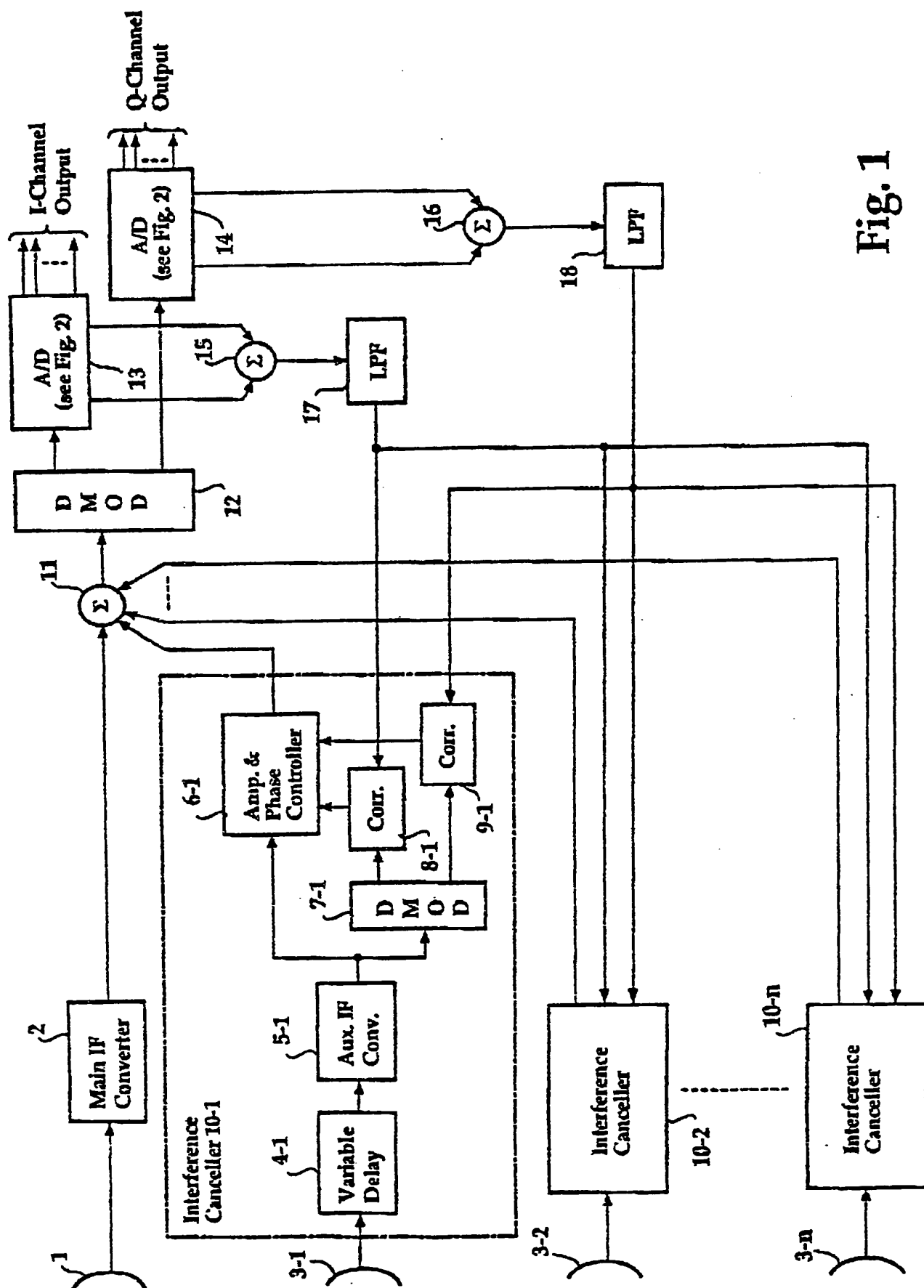
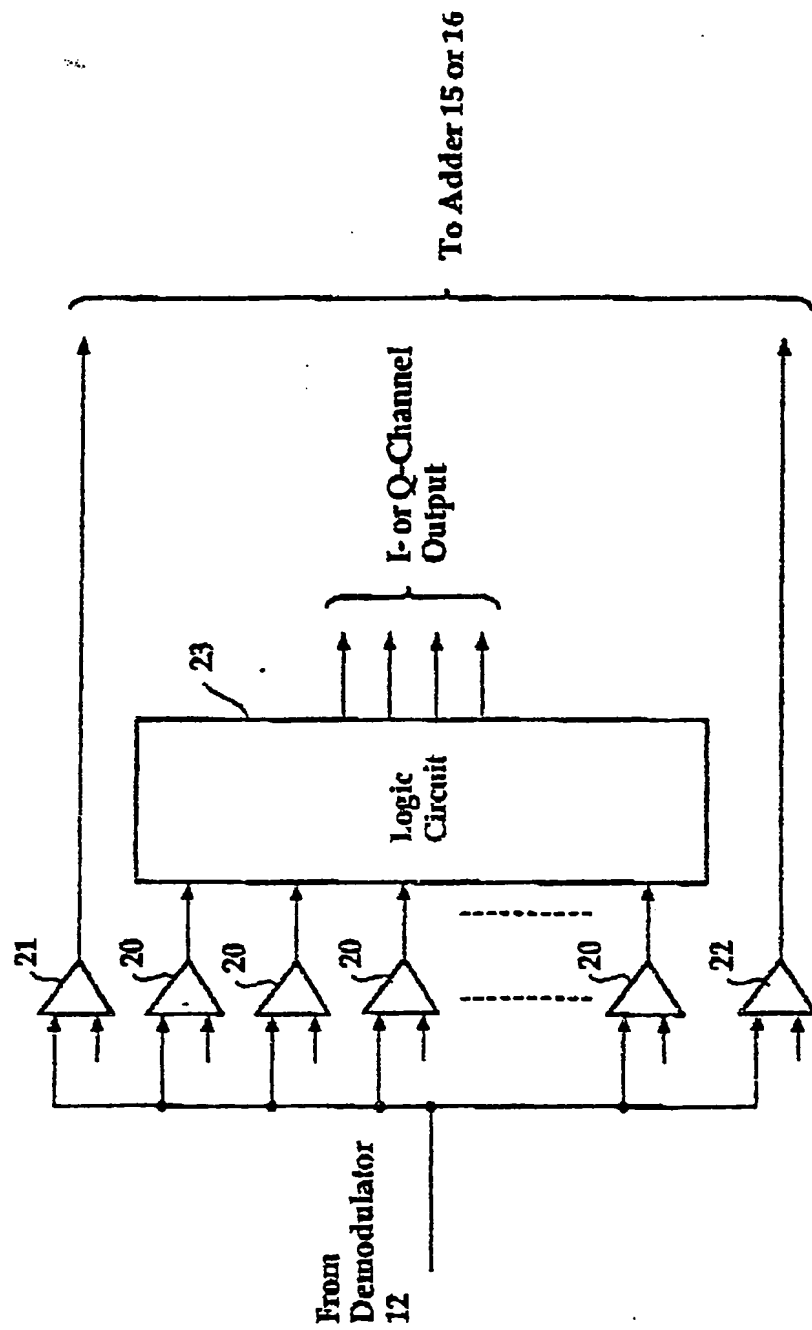
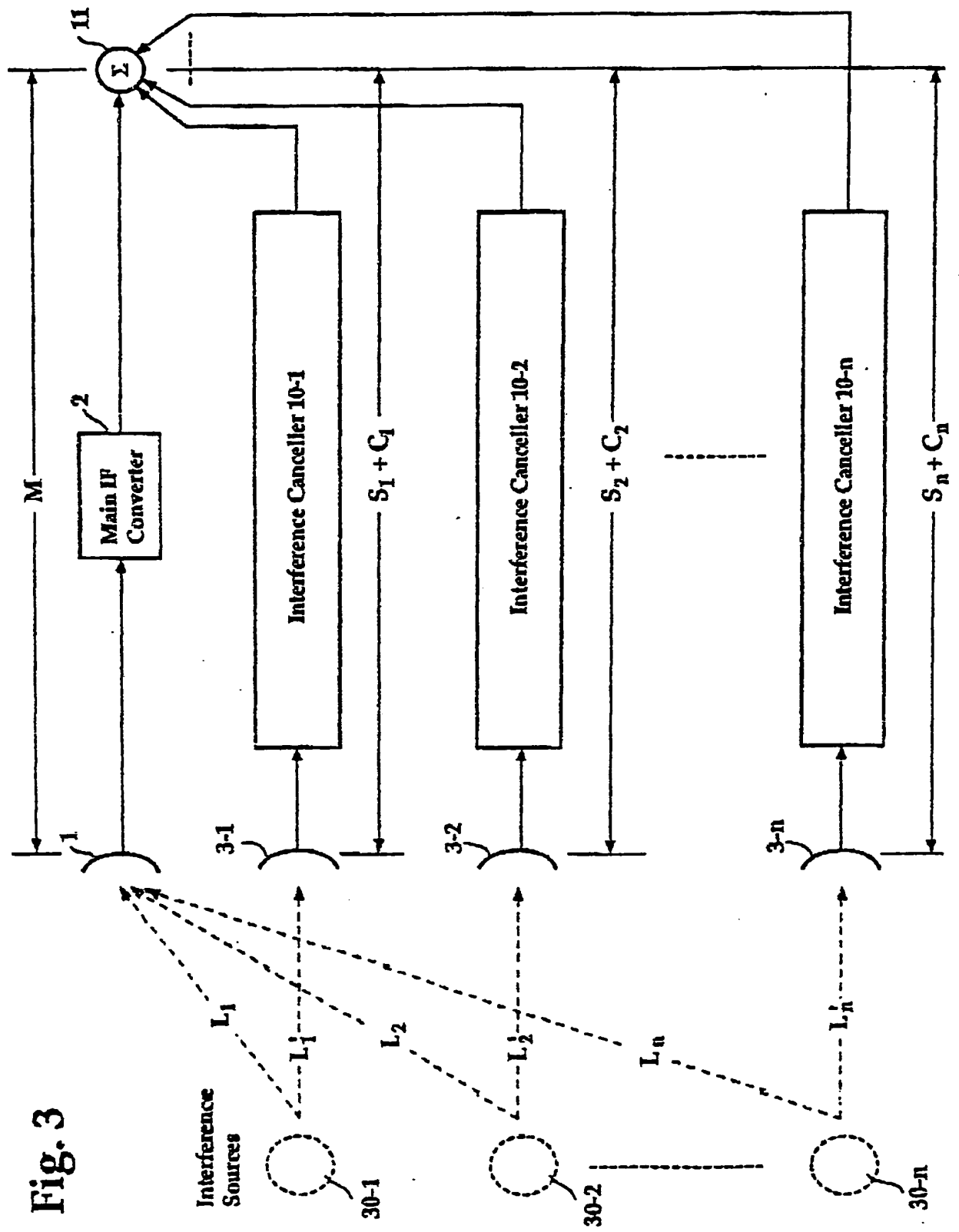


Fig. 1

Fig. 2**A/D Converter 13 (14)**



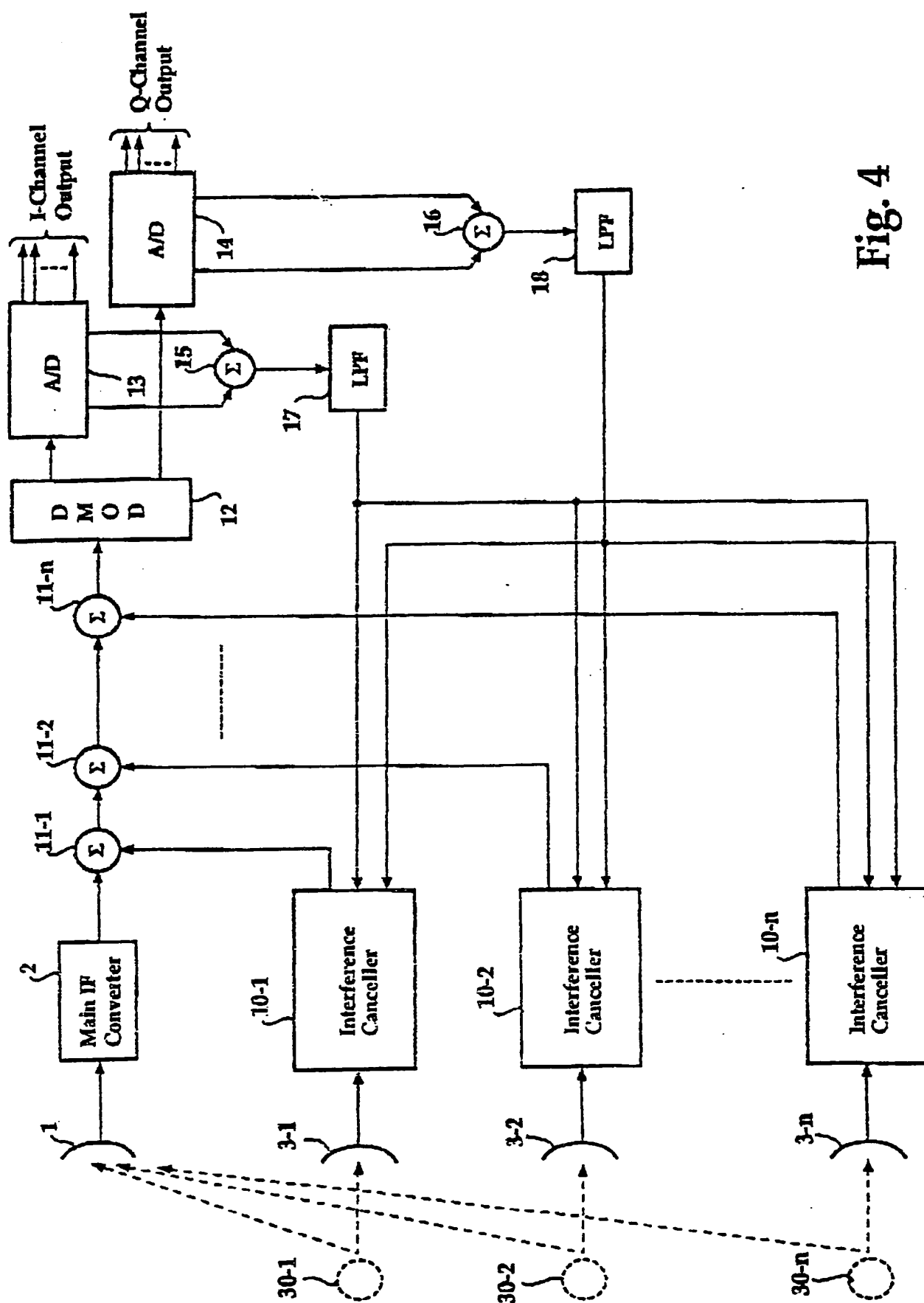
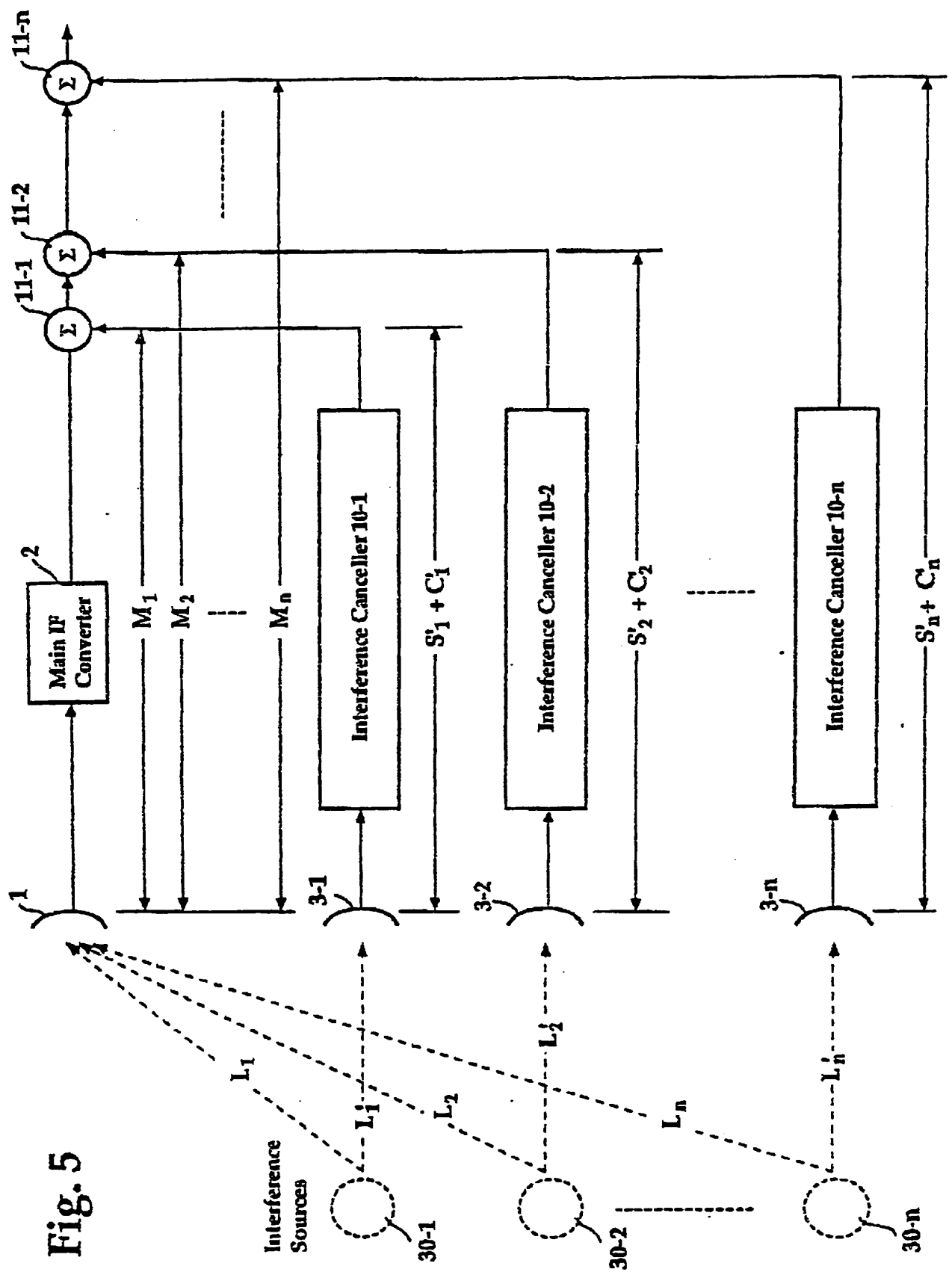


Fig. 4



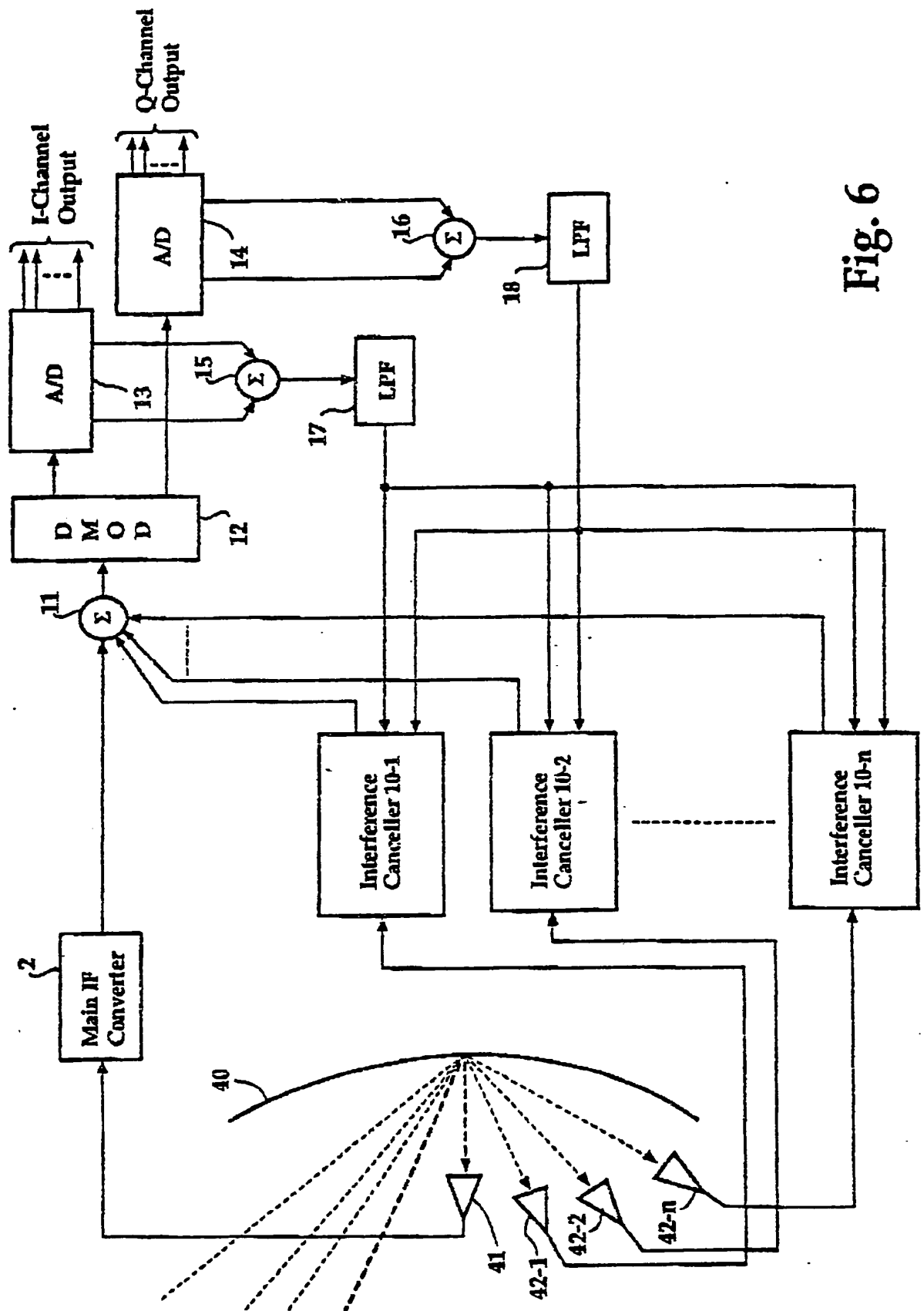


Fig. 6



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(54) Demodulator with multiple interference cancellers responsive to correlations between undesired signals and error signals.

(57) Undesired signals detected by a main antenna (1) are cancelled by corresponding interference cancelling signals. The output of the main antenna is frequency converted to IF region and decomposed into first and second main baseband components. Decision circuits are provided for making a decision on whether each of the first and second main baseband components exceeds each of multiple thresholds and produces multibit codes as well as error signals. Auxiliary antennas (3-1...3-m) respectively detect the undesired signals and feed auxiliary frequency converters (5-1) for translating the frequency of the respective outputs of the auxiliary antennas to the intermediate frequency. Auxiliary quadrature demodulators (7-1) are provided for re-

spectively decomposing the output of each auxiliary frequency converter into first and second auxiliary baseband components. Correlations (8-1,9-1) are detected between the first auxiliary baseband components and the first error signal and between the second auxiliary baseband component and the second error signal. Amplitude and phase controllers (6-1) are responsive to the detected correlations to control the outputs of the auxiliary frequency converters to generate the interference cancelling signals. Variable length delay lines (4-1) are associated respectively with the auxiliary antennas for introducing delays so that both cancelling signals and corresponding interfering components are time-coincident at the summing circuit.

EP 0 371 433 A3

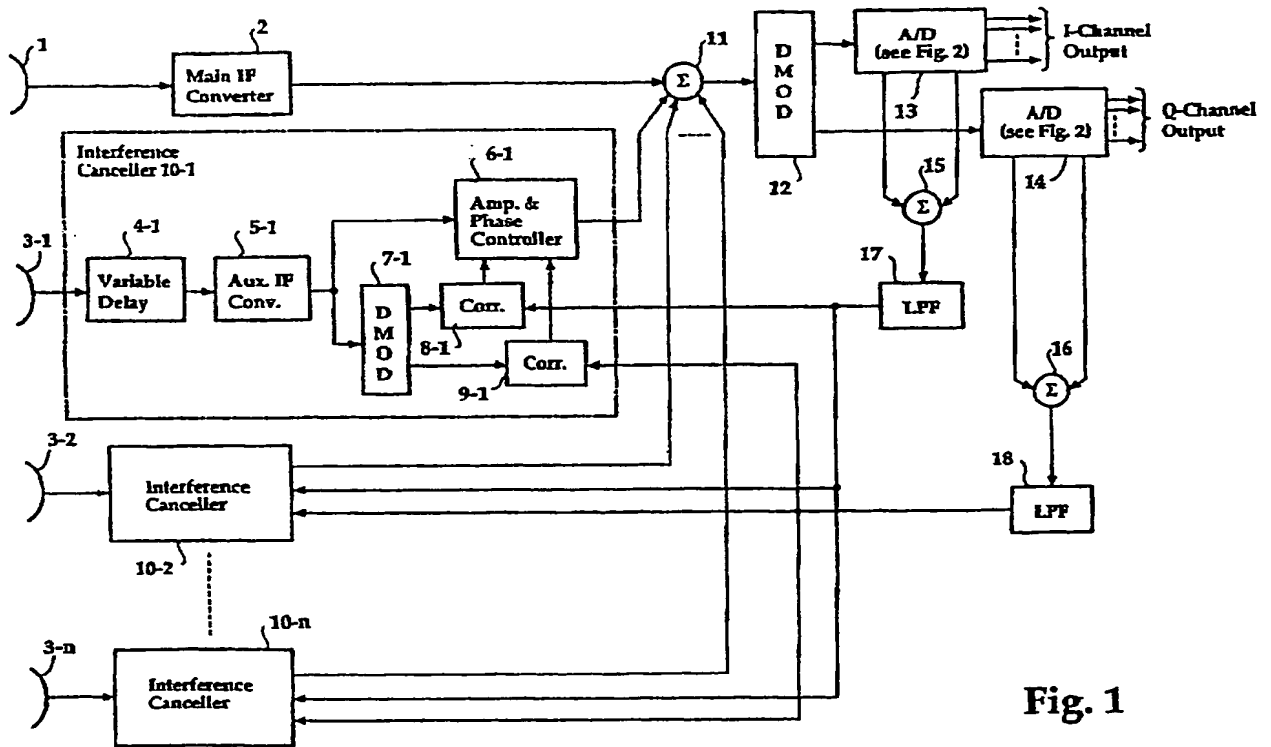


Fig. 1



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EUROPEAN SEARCH REPORT

Application Number

EP 89 12 1880

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 228 786 (NIPPON TELEGRAPH AND TELEPHONE CORP.) * Page 2, lines 34-46; page 6, lines 5-20; page 7, lines 3-18; figures 1,5 *	1	H 04 B 7/005 H 04 B 1/12
A	-----	2,3	
Y	US-A-4 313 116 (POWELL et al.) * Column 2, lines 10-25; claim 1; figure 5 *	1	
A	-----	2	
A	US-A-4 470 138 (GUTLEBER) * Column 4, lines 20-29; figure 3 *	3	

A	PATENT ABSTRACTS OF JAPAN, vol. 9, no. 106 (E-313)[1829], 10th May 1985; & JP-A-59 230 335 (NIPPON DENSHIN DENWA KOSHA) 24-12-1984 * Whole document *		

The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
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The Hague		26 June 91	BOSSEN M.
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